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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,263	04/02/2004	Hong Wang	884.219US2	1794

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/817,263	WANG ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02 April 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Specification as received on 02 April 2004; Abstract as received on 02 April 2004; Drawings as received on 02 April 2004; Oath or Declaration as received on 02 April 2004; Preliminary Amendment as received on 02 April 2004; and IDS as received on 02 April 2004.

Priority

3. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged.

Specification

4. The abstract of the disclosure is objected to because the extra text on the bottom portion of the "Abstract of Disclosure" page. Specifically, the language with regards to the "Express Mail" label number. Please provide a clean copy of the Abstract page without the "Express Mail" label number information on the page. Correction is required. See MPEP § 608.01(b).

5. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

6. The disclosure is objected to because of the following informalities: The specification is missing the "Brief Summary of Invention".

7. Appropriate correction is required.

Information Disclosure Statement

8. The information disclosure statement (IDS) submitted on 02 April 2006 and is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Double Patenting

9. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

10. A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

11. Claims 1-18 and 26-30 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-18 and 26-30 of prior U.S. Patent No. 6,732,260. This is a double patenting rejection. The related claims are laid forth in the table below.

U.S. Patent No. 6,732,260	Instant Application
Claim 1	**Claim 1**
A branch target prefetch apparatus comprising:	A branch target prefetch apparatus comprising:
A presbyopic target buffer configured to receive a presbyopic target buffer record,	A presbyopic target buffer configured to receive a presbyopic target buffer record,
Wherein the presbyopic target buffer record maps an entry location of a first code region to an entry location of a second code region; and	Wherein the presbyopic target buffer record maps an entry location of a first code region to an entry location of a second code region; and
A prefetch stream buffer configured to receive instructions from the second code region responsive to if an instruction pointer is to encounter the entry location of the first code region.	A prefetch stream buffer configured to receive instructions from the second code region responsive to an instruction pointer encountering the entry location of the first code region.
Claim 2	**Claim 2**
The branch target prefetch apparatus of claim 1 wherein the presbyopic target buffer is configured to receive the presbyopic target buffer record responsive to a branch instruction being encountered in the first code region, the branch instruction having a branch target address equal to the entry location of the second code region.	The branch target prefetch apparatus of claim 1 wherein the presbyopic target buffer is configured to receive the presbyopic target buffer record responsive to a branch instruction being encountered in the first code region, the branch instruction having a branch target address equal to the entry location of the second code region.
Claim 3	**Claim 3**
The branch target prefetch apparatus of claim 2 further comprising a branch target buffer configured to receive a branch target buffer record that maps an address of the branch instruction to the entry location of the second code region.	The branch target prefetch apparatus of claim 2 further comprising a branch target buffer configured to receive a branch target buffer record that maps an address of the branch instruction to the entry location of the second code region.
Claim 4	**Claim 4**
The branch target prefetch apparatus of claim 3 wherein the presbyopic target buffer is configured to receive a plurality of presbyopic	The branch target prefetch apparatus of claim 3 wherein the presbyopic target buffer is configured to receive a plurality of presbyopic

target buffer records, and is further configured to be searched recursively.	target buffer records, and is further configured to be searched recursively.
Claim 5	**Claim 5**
The branch target prefetch apparatus of claim 4 wherein the prefetch stream buffer is configured to receive instructions from a plurality of code regions responsive to a recursive search of the presbyopic target buffer.	The branch target prefetch apparatus of claim 4 wherein the prefetch stream buffer is configured to receive instructions from a plurality of code regions responsive to a recursive search of the presbyopic target buffer.
Claim 6	**Claim 6**
The branch target prefetch apparatus of claim 5 wherein the prefetch stream buffer is configured to differentiate between instructions such that instructions from different ones of the plurality of code regions can be invalidated.	The branch target prefetch apparatus of claim 5 wherein the prefetch stream buffer is configured to differentiate between instructions such that instructions from different ones of the plurality of code regions can be invalidated.
Claim 7	**Claim 7**
The branch target prefetch apparatus of claim 3 wherein the branch target buffer record includes a first confidence counter having a first number of bits, and the presbyopic target buffer record includes a second confidence counter having a second number of bits that is greater than the first number of bits.	The branch target prefetch apparatus of claim 3 wherein the branch target buffer record includes a first confidence counter having a first number of bits, and the presbyopic target buffer record includes a second confidence counter having a second number of bits that is greater than the first number of bits.
Claim 8	**Claim 8**
The branch target prefetch apparatus of claim 1 wherein the presbyopic target buffer record is configured to map the entry location of the first code region to entry locations of a plurality of second code regions.	The branch target prefetch apparatus of claim 1 wherein the presbyopic target buffer record is configured to map the entry location of the first code region to entry locations of a plurality of second code regions.
Claim 9	**Claim 9**
The branch target prefetch apparatus of claim 1 wherein a cache memory has a cache latency associated therewith, and the prefetch target buffer has a depth at least as deep as one cache latency.	The branch target prefetch apparatus of claim 1 wherein a cache memory has a cache latency associated therewith, and the prefetch target buffer has a depth at least as deep as one cache latency.
Claim 10	**Claim 10**
A processor comprising:	A processor comprising:
A branch target buffer responsive to fetched instruction addresses,	A branch target buffer responsive to fetched instruction addresses,
Wherein the branch target buffer is configured to map branch instruction addresses to branch target addresses; and	Wherein the branch target buffer is configured to map branch instruction addresses to branch target addresses; and
A presbyopic target buffer responsive to the branch target buffer,	A presbyopic target buffer responsive to the branch target buffer,

Wherein the presbyopic target buffer is configured to map branch target addresses to subsequent branch target addresses.	Wherein the presbyopic target buffer is configured to map branch target addresses to subsequent branch target addresses.
Claim 11	**Claim 11**
The processor of claim 10 further comprising: a stream buffer configured to receive instructions fetched from subsequent branch target addresses specified in the presbyopic target buffer.	The processor of claim 10 further comprising: a stream buffer configured to receive instructions fetched from subsequent branch target addresses specified in the presbyopic target buffer.
Claim 12	**Claim 12**
The processor of claim 10 wherein the presbyopic target buffer is configured to be recursively searched to predict a plurality of subsequent branch target addresses.	The processor of claim 10 wherein the presbyopic target buffer is configured to be recursively searched to predict a plurality of subsequent branch target addresses.
Claim 13	**Claim 13**
The processor of claim 10 wherein the presbyopic target buffer implements skip-adjacent mapping.	The processor of claim 10 wherein the presbyopic target buffer implements skip-adjacent mapping.
Claim 14	**Claim 14**
The processor of claim 10 wherein a complete branch target address is specified by a fixed number of bits, and the presbyopic target buffer includes mapping records that specify branch target addresses using less than the fixed number of bits.	The processor of claim 10 wherein a complete branch target address is specified by a fixed number of bits, and the presbyopic target buffer includes mapping records that specify branch target addresses using less than the fixed number of bits.
Claim 15	**Claim 15**
A processor comprising:	A processor comprising:
A branch target buffer responsive to fetched instruction addresses,	A branch target buffer responsive to fetched instruction addresses,
Wherein the branch target buffer is configured to be searched for the fetched instruction addresses and corresponding branch target addresses;	Wherein the branch target buffer is configured to be searched for the fetched instruction addresses and corresponding branch target addresses;
A presbyopic target buffer responsive to the branch target buffer,	A presbyopic target buffer responsive to the branch target buffer,
Wherein the presbyopic target buffer is configured to be searched for subsequent dynamic blocks as a function of branch target addresses.	Wherein the presbyopic target buffer is configured to be searched for subsequent dynamic blocks as a function of branch target addresses.
Claim 16	**Claim 16**
The processor of claim 15 wherein the presbyopic target buffer is configured to map branch target addresses to subsequent dynamic block exit addresses.	The processor of claim 15 wherein the presbyopic target buffer is configured to map branch target addresses to subsequent dynamic block exit addresses.

Claim 17	**Claim 17**
The processor of claim 16 wherein the branch target buffer is further responsive to subsequent dynamic block exit addresses from the presbyopic target buffer.	The processor of claim 16 wherein the branch target buffer is further responsive to subsequent dynamic block exit addresses from the presbyopic target buffer.
Claim 18	**Claim 18**
The processor of claim 17 wherein the branch target buffer and presbyopic target buffer are configured to be searched recursively in combination.	The processor of claim 17 wherein the branch target buffer and presbyopic target buffer are configured to be searched recursively in combination.
Claim 26	**Claim 26**
A method comprising:	An instruction prefetch method comprising:
In a first buffer that maps branch instruction addresses to block entry addresses, searching for a first buffer record having a branch instruction address that matches a current instruction address;	In a first buffer that maps branch instruction addresses to block entry addresses, searching for a first buffer record having a branch instruction address that matches a current instruction address;
After the first buffer record is found, searching a second buffer that maps block entry addresses to subsequent block entry addresses for a second buffer record having a block entry address matching the first buffer record; and	When the first buffer record is found, searching a second buffer that maps block entry addresses to subsequent block entry addresses for a second buffer record having a block entry address matching the first buffer record; and
After the second buffer record is found, prefetching instructions beginning at a subsequent block entry address included in the second buffer record.	When the second buffer record is found, prefetching instructions beginning at a subsequent block entry address included in the second buffer record.
Claim 27	**Claim 27**
The method of claim 26 wherein prefetching comprises entering instructions into a stream buffer, the stream buffer having a coloring field for each instruction entered.	The method of claim 26 wherein prefetching comprises entering instructions into a stream buffer, the stream buffer having a coloring field for each instruction entered.
Claim 28	**Claim 28**
The method of claim 26 further comprising:	The method of claim 26 further comprising:
Searching the second buffer recursively; and	Searching the second buffer recursively; and
For each matching record found in the second buffer, each matching record having a corresponding subsequent block entry address, prefetching instructions from each of the corresponding subsequent block entry addresses.	For each matching record found in the second buffer, each matching record having a corresponding subsequent block entry address, prefetching instructions from each of the corresponding subsequent block entry addresses.
Claim 29	**Claim 29**
The method of claim 28 wherein prefetching comprises:	The method of claim 28 wherein prefetching comprises:

Entering instructions into a stream buffer, the stream buffer having a coloring field for each instruction entered; and	Entering instructions into a stream buffer, the stream buffer having a coloring field for each instruction entered; and
Assigning a different color to instructions fetched from different subsequent block entry addresses.	Assigning a different color to instructions fetched from different subsequent block entry addresses.
Claim 30	**Claim 30**
The method of claim 29 wherein each recursive search represents a predicted branch,	The method of claim 29 wherein each recursive search represents a predicted branch,
The method further comprising flushing from the stream buffer instructions prefetched as a result of a mispredicted branch	The method further comprising flushing from the stream buffer instructions prefetched as a result of a mispredicted branch.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

12. Claims 19-25 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 19-21 and 23-25 of U.S. Patent No. 6,732,260 (herein referred to as '260). Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of '260 are narrower and are overlapped

by the broader claim language of the instant application. The related claims are laid forth in the table below. The similar claim limitations are underlined and/or italicized.

U.S. Patent No. 6,732,260	Instant Application
Claim 19	**Claim 19**
A processor comprising:	A processor comprising:
A first fetch buffer configured to receive instructions prefetched from predicted branch target addresses; and	A first fetch buffer configured to receive instructions prefetched from predicted branch target addresses; and
A second fetch buffer configured to receive instructions prefetched from predicted subsequent blocks,	A second fetch buffer configured to receive instructions prefetched from predicted subsequent blocks.
Responsive to if an instruction pointer in the processor is to point to an entry location of a block of instructions, based on a presbyopic target buffer record that maps entry location of the block of instructions to entry locations of the predicted subsequent blocks.	
Claim 20	**Claim 20**
The processor of claim 19 wherein the second fetch buffer includes a coloring field for each instruction included therein, such that each instruction included therein can be assigned a color.	The processor of claim 19 wherein the second fetch buffer includes a coloring field for each instruction included therein, such that each instruction included therein can be assigned a color.
Claim 21	**Claim 21**
The processor of claim 19 wherein the second fetch buffer includes a subsequent block demarcation mechanism to distinguish prefetched instructions from different predicted subsequent blocks.	The processor of claim 19 wherein the second fetch buffer includes a subsequent block demarcation mechanism to distinguish prefetched instructions from different predicted subsequent blocks.
Claim 22	**Claim 22**
The processor of claim 19 further including a branch target buffer having records that when populated, map branches to predicted branch targets.	The processor of claim 19 further including a branch target buffer having records that when populated, map branches to predicted branch targets.
Claim 19 (excerpt)	**Claim 23**
Responsive to if an instruction pointer in the processor is to point to an entry location of a block of instructions, based on a presbyopic target buffer record that maps entry location of the block of instructions to entry locations of the predicted subsequent blocks.	The processor of claim 22 further including a presbyopic target buffer having records that when populated, map predicted branch target addresses to predicted subsequent blocks.

Claim 24	Claim 24
The processor of claim 23 wherein the presbyopic target buffer maps each predicted branch target address to a plurality of predicted subsequent blocks.	The processor of claim 23 wherein the presbyopic target buffer maps each predicted branch target address to a plurality of predicted subsequent blocks.
Claim 25	**Claim 25**
The processor of claim 23 wherein the presbyopic target buffer is configured to be recursively searched.	The processor of claim 23 wherein the presbyopic target buffer is configured to be recursively searched.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 19 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar, U.S. Number 5,506,976 (herein referred to as Jaggar) in view of Yeh et al., U.S. Number 5,742,804 (herein referred to as Yeh).

15. Referring to claim 19, Jaggar has taught a processor comprising:

a. A first fetch buffer configured to receive instructions from predicted branch target addresses (Jaggar column 2, lines 30-38); and

b. A second fetch buffer configured to receive instructions from predicted subsequent blocks (Jaggar column 2, lines 20-28 and 59-60)

16. Jaggar has not taught the instructions were prefetched. Yeh has taught prefetching instructions (Yeh column 1, lines 23-29 and column 2, lines 49-55). A person of ordinary skill in the art at the time the invention was made, and as recognized in Yeh, would have recognized that prefetching decreases the instruction fetch penalty (Yeh column 1, lines 39-44). Therefore, it

would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the prefetch of Yeh in the device of Jaggar to decrease the amount of time needed to fetch an instruction.

17. Referring to claim 21, Jaggar in view of Yeh has taught wherein the second fetch buffer includes a subsequent block demarcation mechanism to distinguish prefetched instructions from different predicted subsequent blocks (Jaggar column 1, lines 34-41). In regards to Jaggar, in order to distinguish between the branches, each branch has a different tag.

18. Referring to claim 22, Jaggar in view of Yeh has taught a branch target buffer having records that when populated, map branches to predicted branch targets (Jaggar column 2, lines 30-38; column 6, lines 57-61; and Figure 2, elements 18 and 20).

19. Referring to claim 23, Jaggar in view of Yeh has taught a presbyopic target buffer having records that when populated, map predicted branch target addresses to predicted subsequent blocks (Jaggar column 2, lines 30-38 and 40-48; column 3, lines 5-8; column 6, lines 57-61; and Figure 2, elements 4, 12, and 16).

20. Referring to claim 24, Jaggar in view of Yeh has taught wherein the presbyopic target buffer maps each predicted branch target address to a plurality of predicted subsequent blocks (Jaggar column 2, lines 40-48 and column 9, lines 8-14).

21. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Yeh as applied to claims 19 and 26 above, and further in view of Papadopoulos, U.S. Patent Number 5,412,799 (herein referred to as Papadopoulos). Jaggar in view of Yeh has not taught wherein the second fetch buffer includes a coloring field for each instruction included therein, such that each instruction included therein can be assigned a color. Papadopoulos has taught

wherein the second fetch buffer includes a coloring field for each instruction included therein, such that each instruction included therein can be assigned a color (Papadopoulos columns 10-11, lines 61-7). A person of ordinary skill in the art at the time the invention was made, and as recognized by Papadopoulos, would have recognized that coloring fields benefits performance tuning and program analysis (Papadopoulos column 10, lines 60-61). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the coloring field of Papadopoulos in the device of Jaggar to improve performance tuning and program analysis.

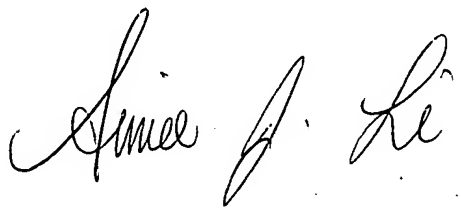
22. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Yeh as applied to claim 23 above, and further in view of Microsoft® Computer Dictionary Fourth Edition by Microsoft Corporation (herein referred to as Microsoft). Jaggar in view of Yeh has taught wherein the presbyopic target buffer is configured to be searched. (Jaggar column 6, lines 55-62). In regards to Jaggar, the branch cache has multiple records, which must be searched for the correct branch. Jaggar in view of Yeh has not taught recursive searching. Microsoft has taught recursion (Microsoft page 377, listing recursion). A person of ordinary skill in the art at the time the invention was made would have recognized that recursion allows for the search routine to be smaller and simpler. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate recursion in the search routing for smaller and simpler routines.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



AJL
Aimee J. Li
14 November 2006